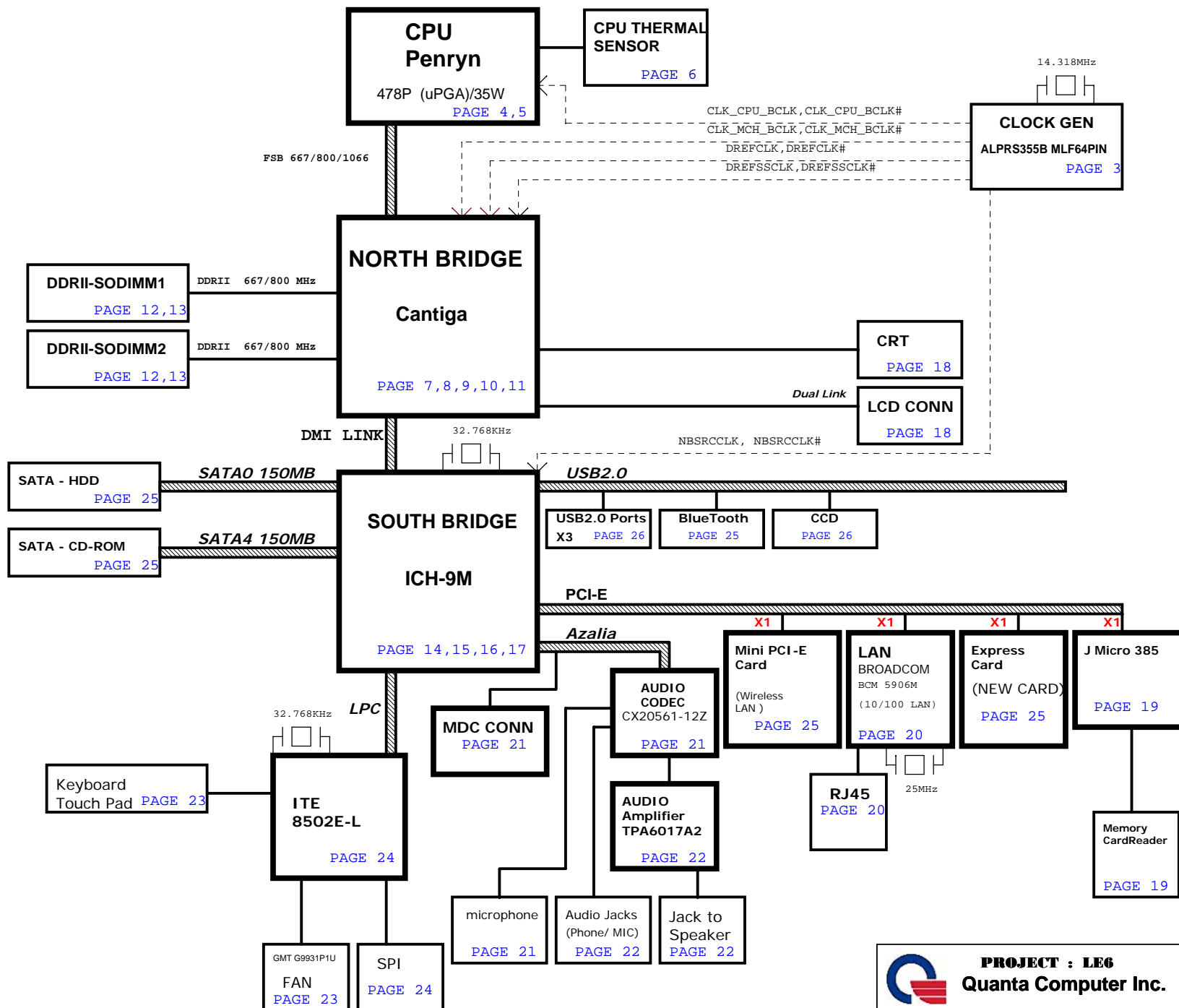


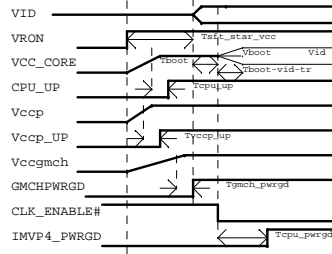
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



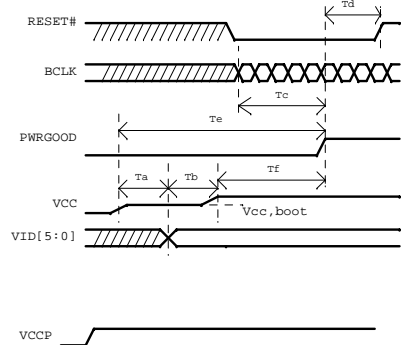
PCB Layers

- Layer 1 TOP
- Layer 2 GND
- Layer 3 IN1
- Layer 4 IN2
- Layer 5 SVCC
- Layer 6 BOTTOM

Power On Sequencing Timing Diagram



YONAH Power-up Timing Specifications

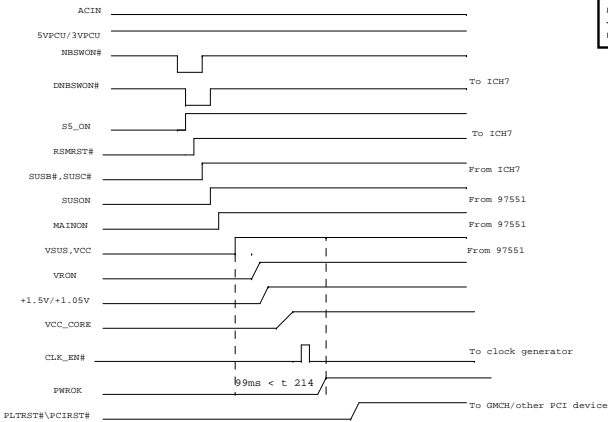


Ta=VCC and VCCP assertion to VID[5:0] valid
Tb=VID[5:0] stable to VCC valid
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot valid to PWRGOOD assertion time

Voltage Rails

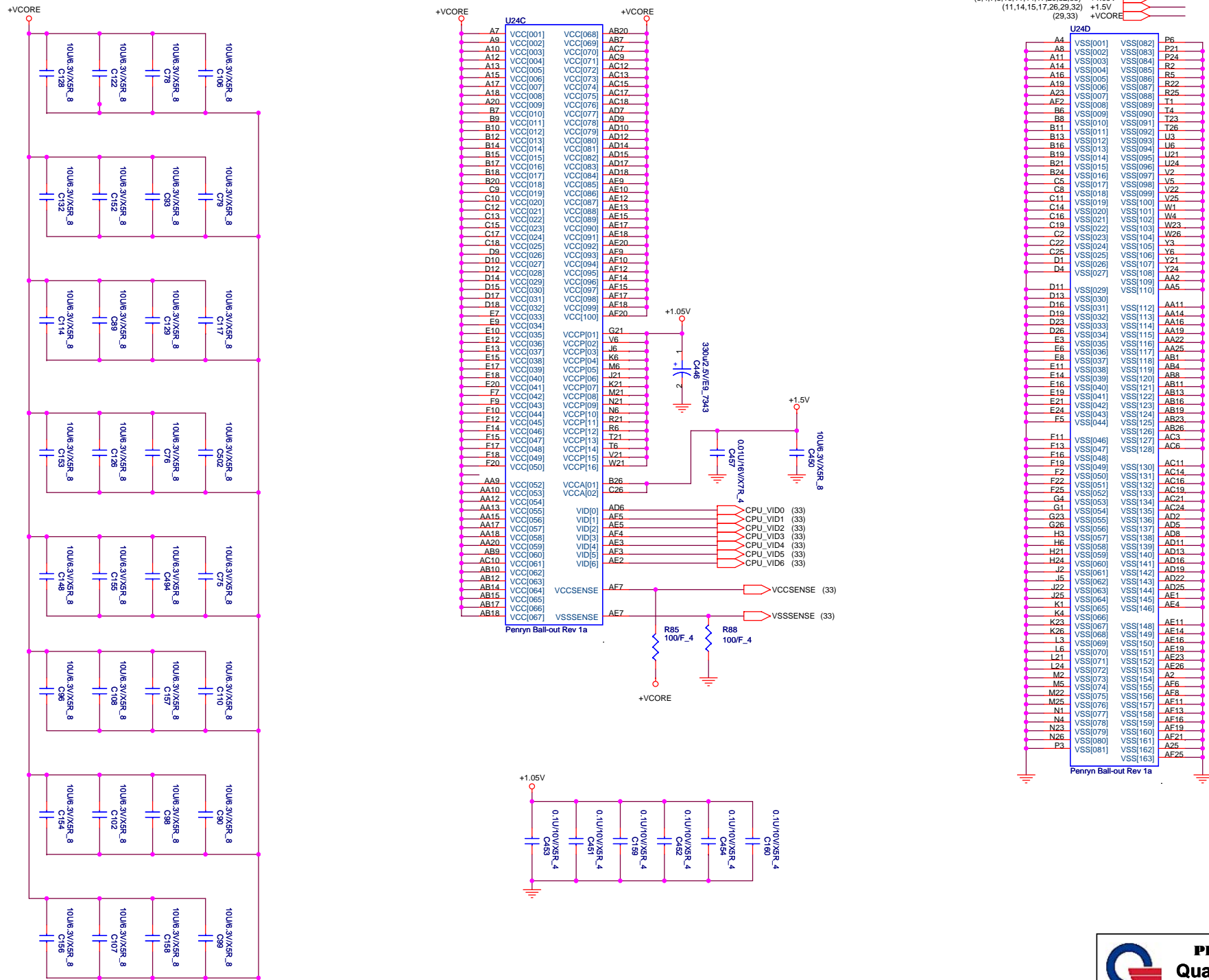
Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5/1.5V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.8VSUS	X	X			SUSON
SMDDR_VTERM/+2.5V/+3V/+5V/+12V	X				MAINON
+VCC_GFX_CORE/+1.2V_GFX_PCIE	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

ACIN POWER ON TIMING

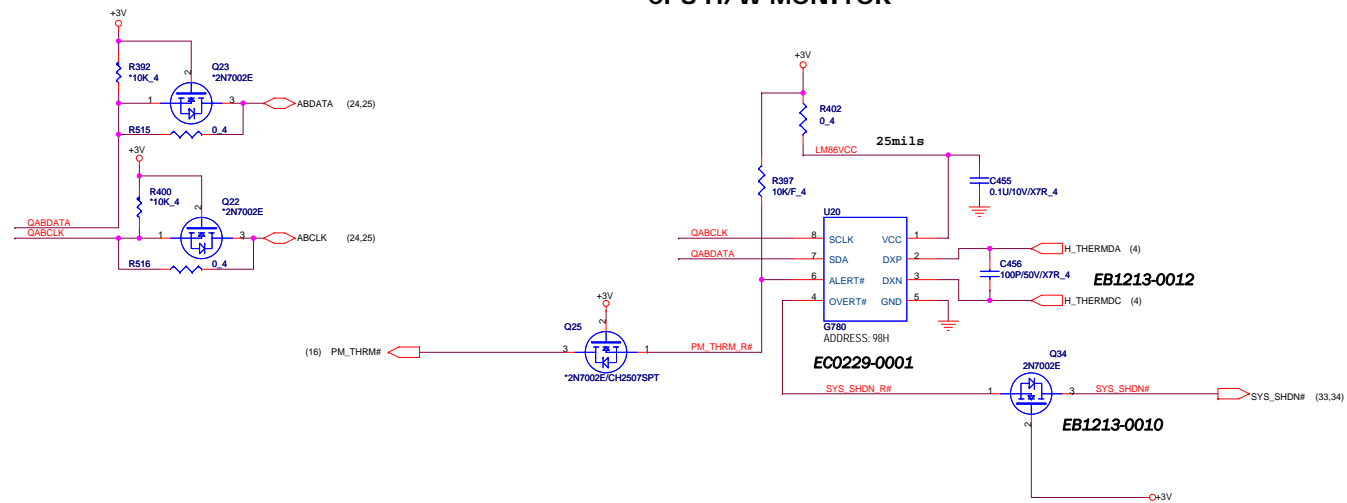


PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
RICHES2	AD25	REQ0# / GNT0#	INT 6# / 7#

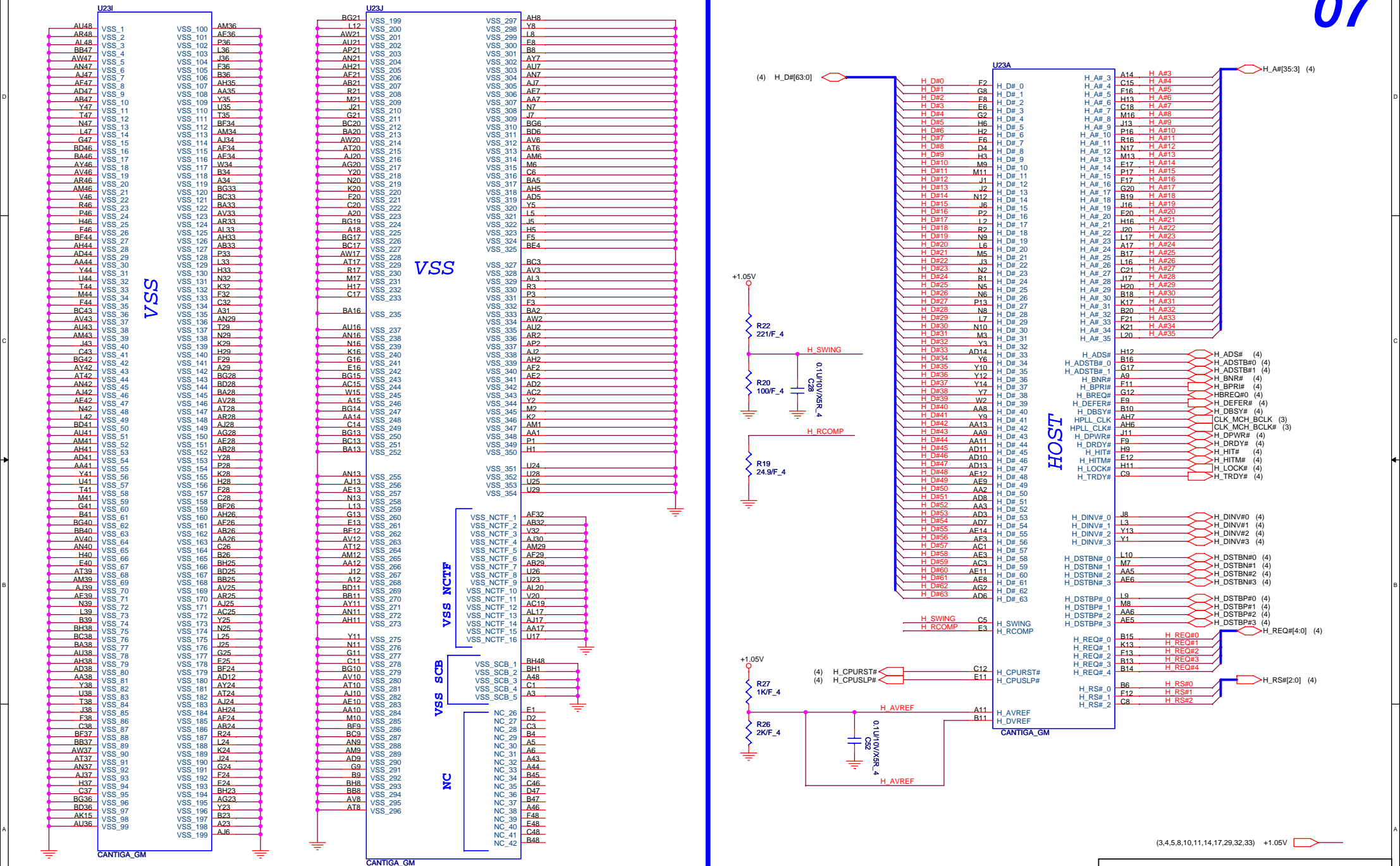




CPU H/W MONITOR



EB1213-0011



MCH_CFG_5 DMix2 selection

Low: DMix2
High: DMix4 (Default)
MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)
MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)
MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved
MCH_CFG_6 ITPM Host Interface

Low: ITPM Host Interface enabled
High: ITPM Host Interface disabled (Default)
MCH_CFG_7 Intel (R) Management Engine Crypto

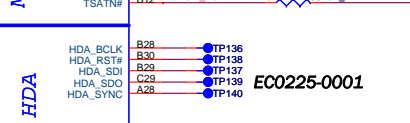
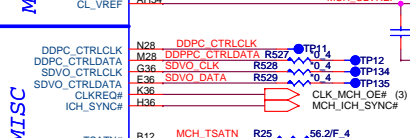
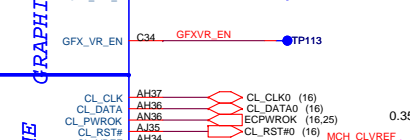
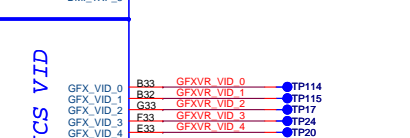
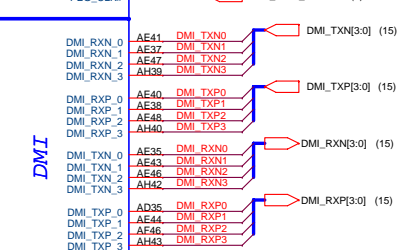
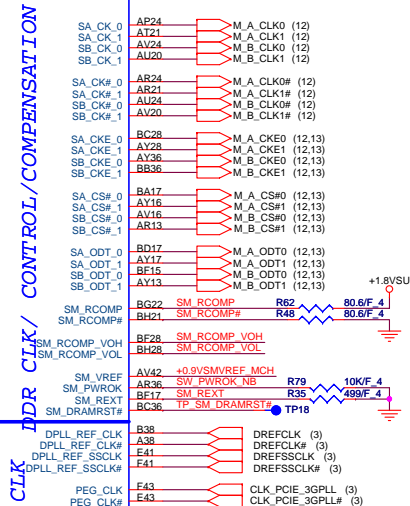
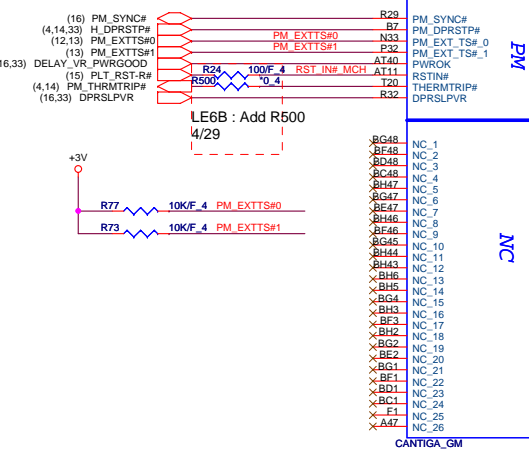
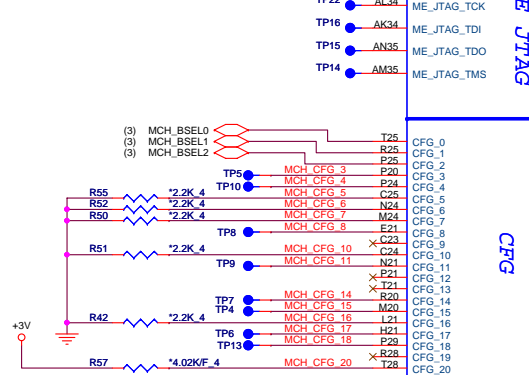
Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

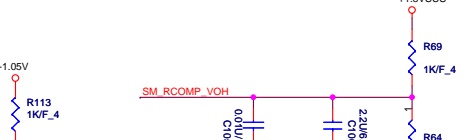
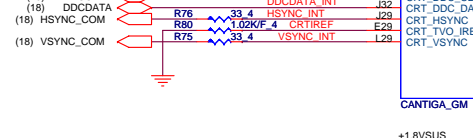
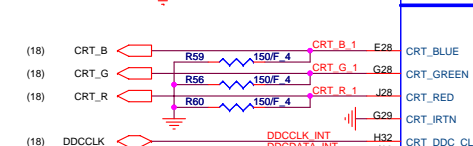
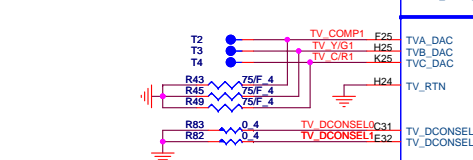
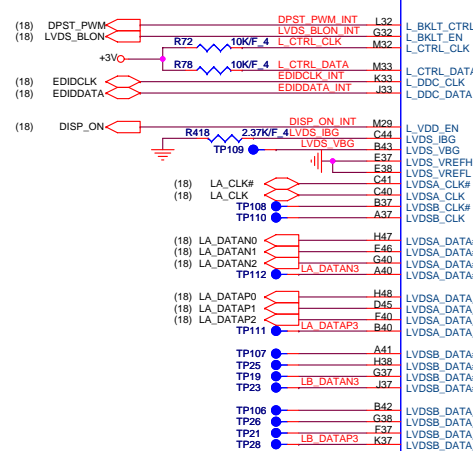
Low: Enabled
High: Disabled (Default)
MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13 MCH_CFG_12 Configuration

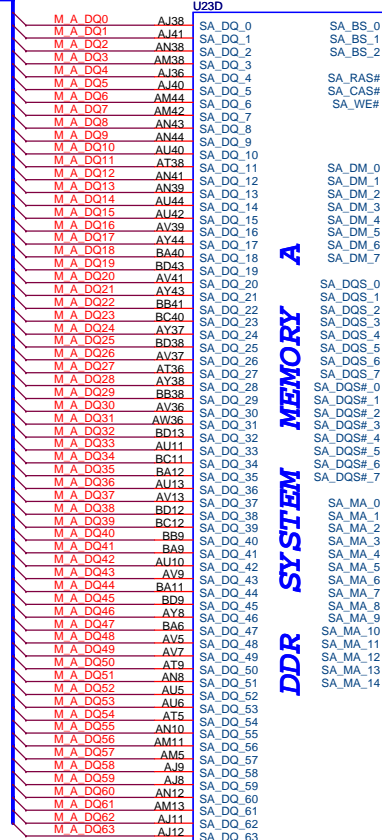
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)



(3,6,11,12,13,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34) +3V
(10,11,12,29,31,32) +1.8VSUS
(3,4,5,7,10,11,14,17,29,32,33) +1.05V
(11) +1.05V_PEG



(12) M_A_DQ[63:0]



CANTIGA_GM

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2
SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7
SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BD21
BG18
AT25
BB20
BD20
AY20

AM37 M A DM0
AT41 M A DM1
AY41 M A DM2
AU39 M A DM3
BB12 M A DM4
AY6 M A DM5
AT7 M A DM6
AJ5 M A DM7

AJ44 M A DQS0
AT44 M A DQS1
BA43 M A DQS2
BC37 M A DQS3
AW12 M A DQS4
BC8 M A DQS5
AU8 M A DQS6
AM7 M A DQS7

AJ43 M A DQS#0
AT43 M A DQS#1
BA44 M A DQS#2
BD37 M A DQS#3
AY12 M A DQS#4
BD8 M A DQS#5
AU9 M A DQS#6
AM8 M A DQS#7

BA21 M A A0
BC24 M A A1
BG24 M A A2
BH24 M A A3
BG25 M A A4
BA24 M A A5
BD24 M A A6
BG27 M A A7
BF25 M A A8
AW24 M A A9
BC21 M A A10
BG26 M A A11
BH26 M A A12
BH17 M A A13
AY25 M A A14

M_A_BS#0 (12,13)
M_A_BS#1 (12,13)
M_A_BS#2 (12,13)
M_A_RAS# (12,13)
M_A_CAS# (12,13)
M_A_WE# (12,13)

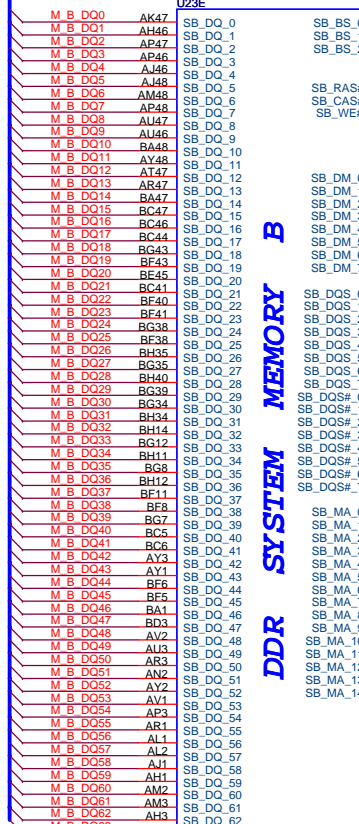
M_A_DM[7:0] (12)

M_A_DQS[7:0] (12)

M_A_DQS#[7:0] (12)

M_A_A[14:0] (12,13)

(12) M_B_DQ[63:0]



CANTIGA_GM

DDR SYSTEM MEMORY B

SB_BS_0
SB_BS_1
SB_BS_2
SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7
SB_DQS#_0
SB_DQS#_1
SB_DQS#_2
SB_DQS#_3
SB_DQS#_4
SB_DQS#_5
SB_DQS#_6
SB_DQS#_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

BC16
BB17
BB33
AU17
BG16
BF14

AM47 M B DM0
AY47 M B DM1
BD40 M B DM2
BF35 M B DM3
BG11 M B DM4
BA3 M B DM5
AP1 M B DM6
AK2 M B DM7

AL47 M B DQS0
AV48 M B DQS1
BG41 M B DQS2
BG37 M B DQS3
BH8 M B DQS4
BB2 M B DQS5
AU1 M B DQS6
AN6 M B DQS7

AL46 M B DQS#0
AV47 M B DQS#1
BH41 M B DQS#2
BH37 M B DQS#3
BG9 M B DQS#4
BC2 M B DQS#5
AN5 M B DQS#6
AN5 M B DQS#7

AV17 M B A0
BA25 M B A1
BC25 M B A2
AU25 M B A3
AW25 M B A4
BB28 M B A5
AU28 M B A6
AW28 M B A7
AT33 M B A8
BD33 M B A9
BB16 M B A10
AW33 M B A11
AY33 M B A12
BH15 M B A13
AU33 M B A14

M_B_BS#0 (12,13)
M_B_BS#1 (12,13)
M_B_BS#2 (12,13)
M_B_RAS# (12,13)
M_B_CAS# (12,13)
M_B_WE# (12,13)

M_B_DM[7:0] (12)

M_B_DQS[7:0] (12)

M_B_DQS#[7:0] (12)

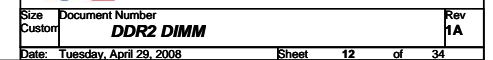
M_B_A[14:0] (12,13)



PROJECT : LE6
Quanta Computer Inc.

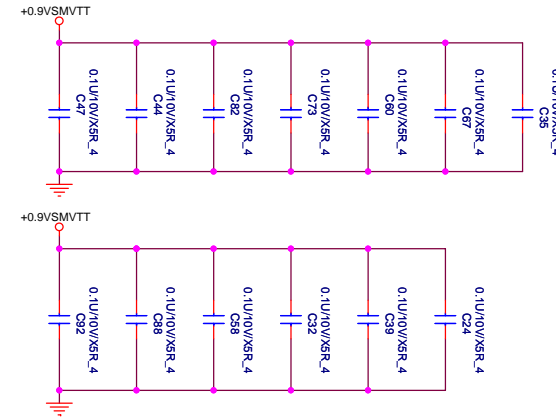
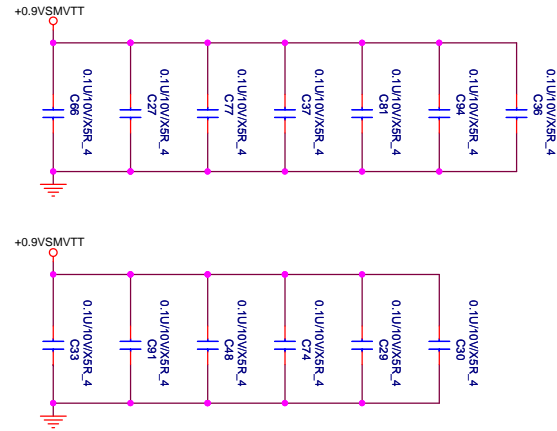




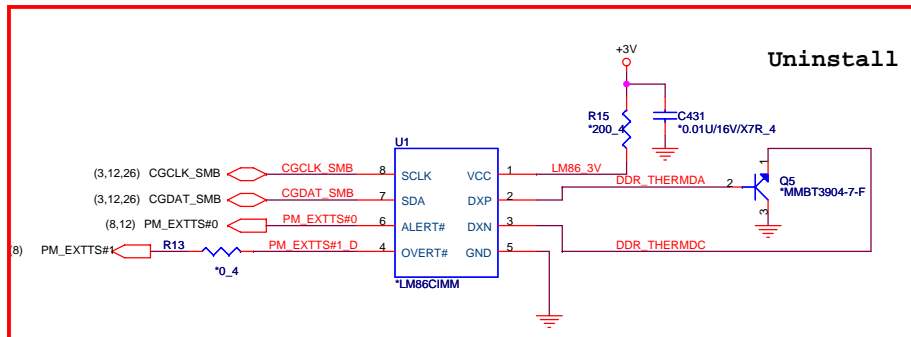
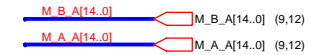
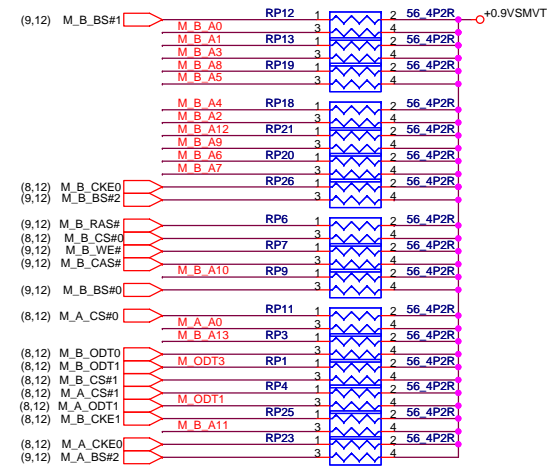
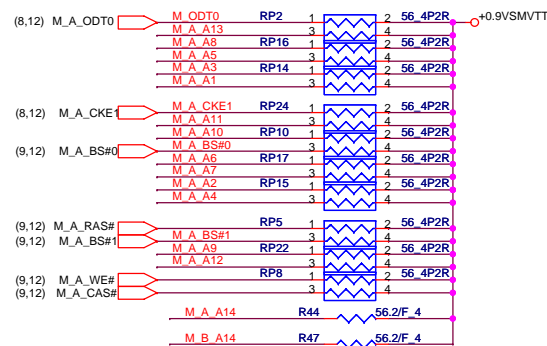


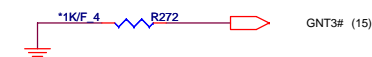
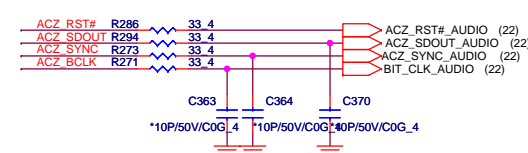
13

DDR II B CHANNEL



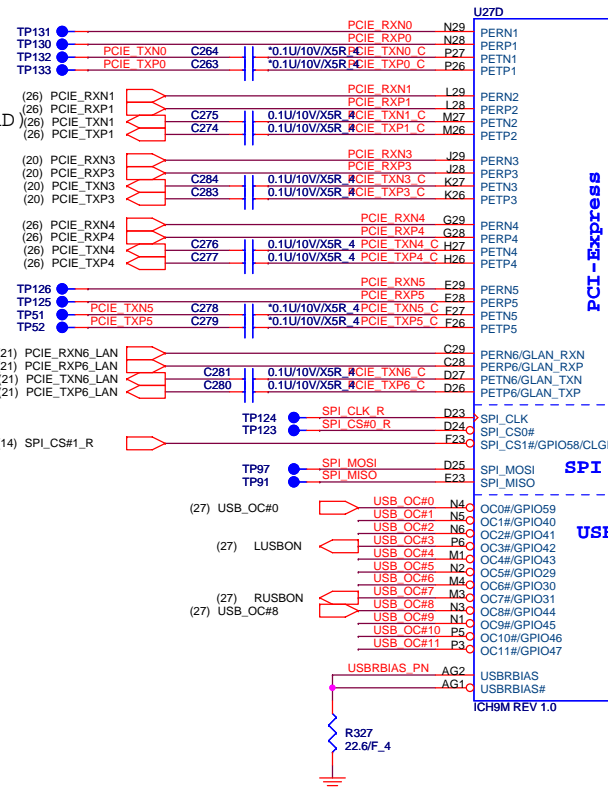
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM







EC0225-0004



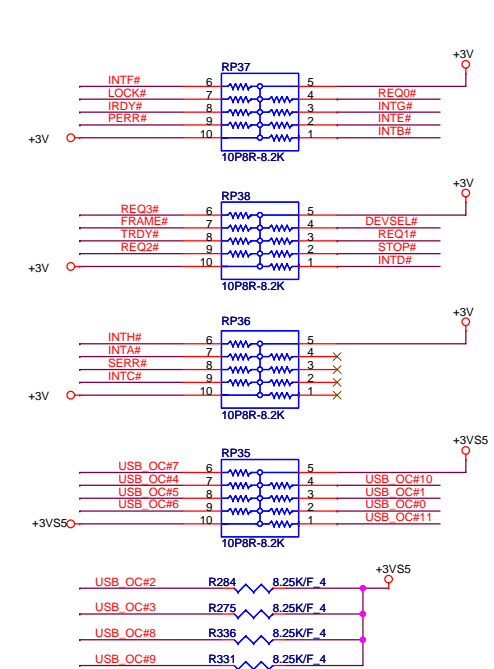
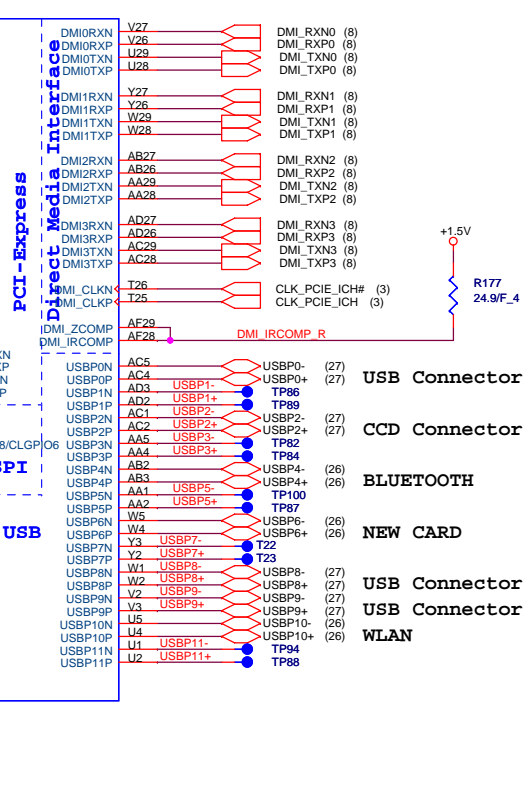
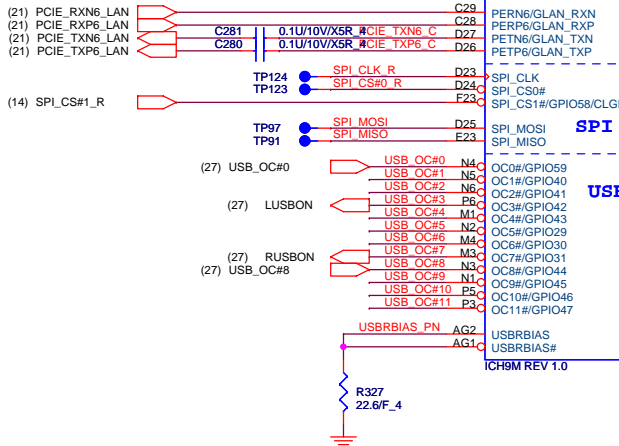
EXPRESS CARD (NEW CARD)

CRAD READER PCI-E

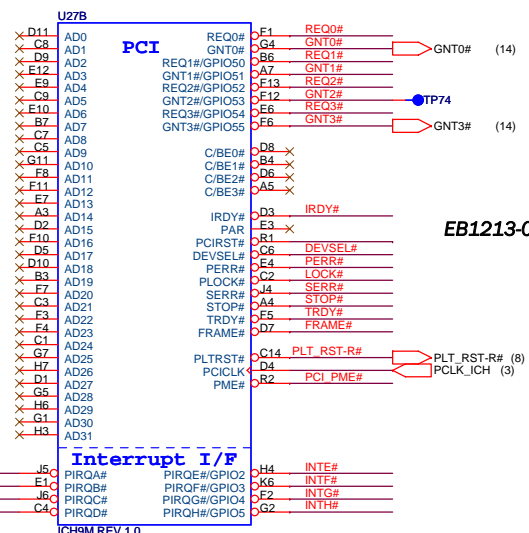
MINI CARD PCI-E(WLAN)

EC0225-0003

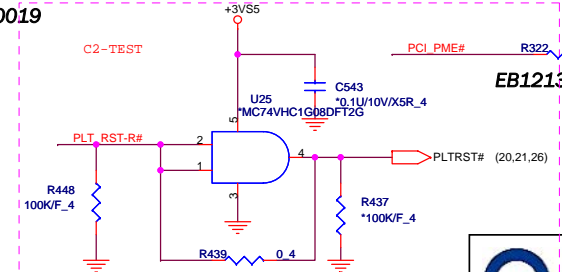
PCI-E-LAN



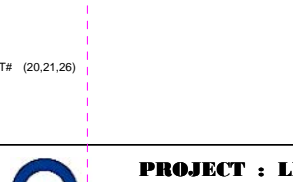
LE6B: Delete HDMI SPI flash IC and relate circuit
2008-4-24



EB1213-0019

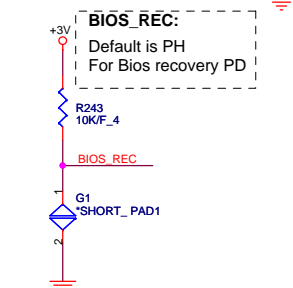


EB1213-0020



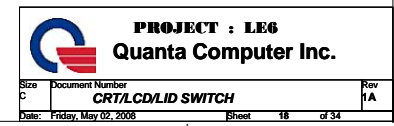
PROJECT : LE6
Quanta Computer Inc.

Size: Custom
Document Number: ICH9-M PCIE 2/4
Date: Friday, May 02, 2008
Sheet: 15 of 34
Rev: 1A



EB1213-0004



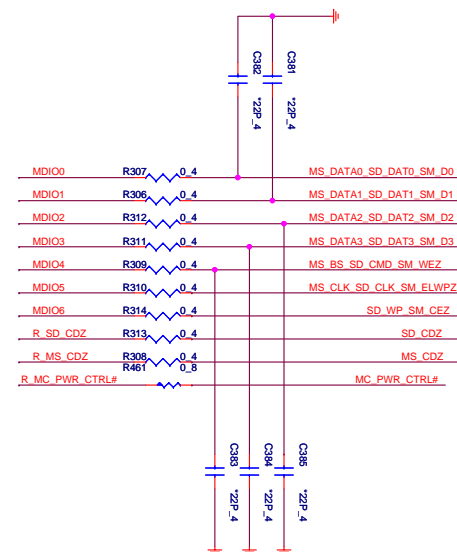


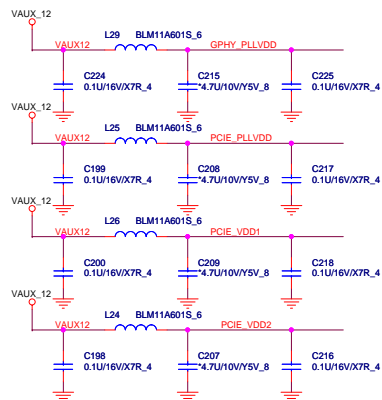
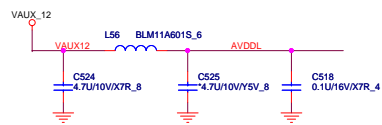
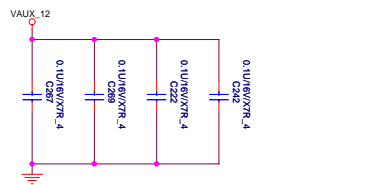
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		PROJECT : LE6 Quanta Computer Inc.	
Size	Document Number	Rev	
Custom	PS8101 & HDMI CONN	1A	
Date: Wednesday, April 23, 2008		Sheet	19 of 34

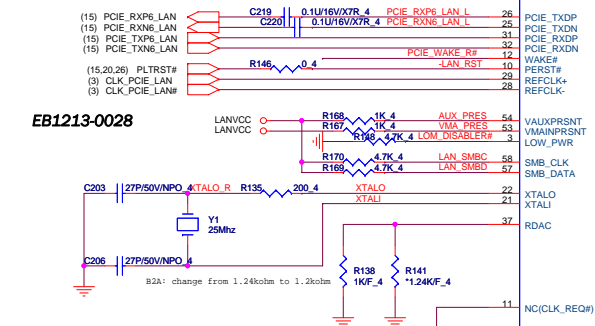


The schematic shows the input stage connected to VCC_XD. It includes a resistor R467 (100K_4) in series with a capacitor C572 (4.7Ue-9/XSR_6). This is followed by a parallel combination of a capacitor C573 (0.01uF/vX/R_4) and a resistor CS68 (0.01uF/vX/R_4).

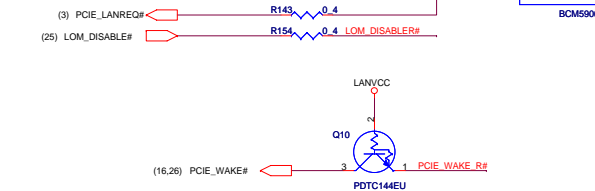




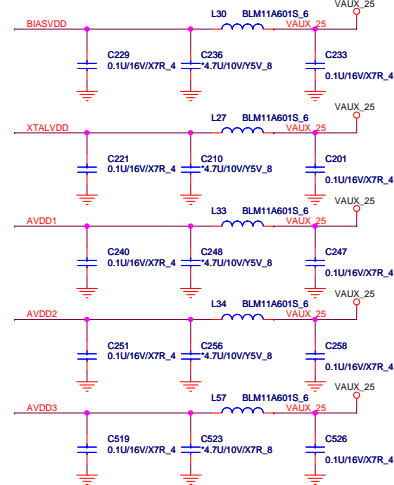
EB1213-0027



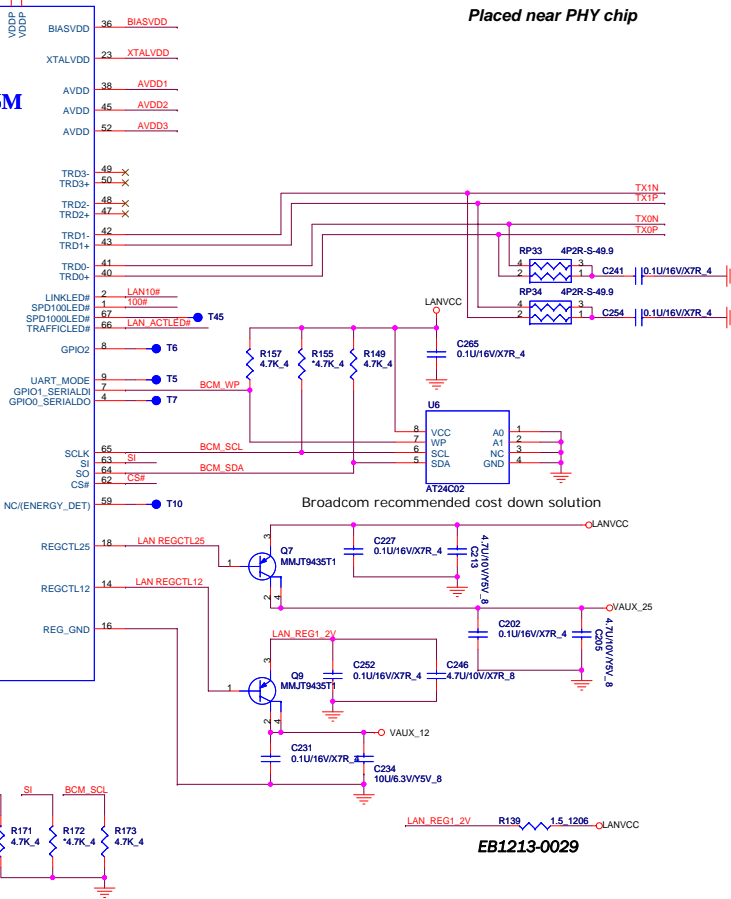
EB1213-0028



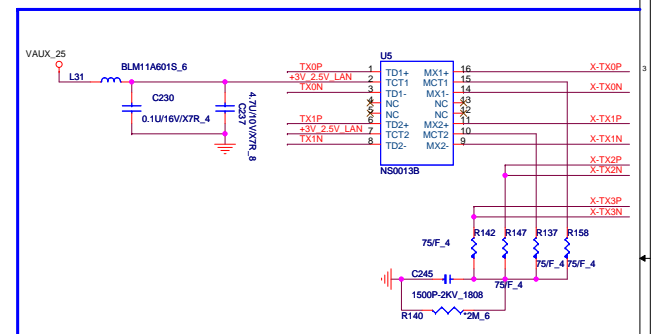
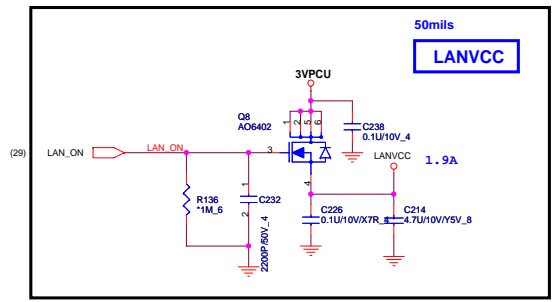
(16,26) PCIE_WAKE# 



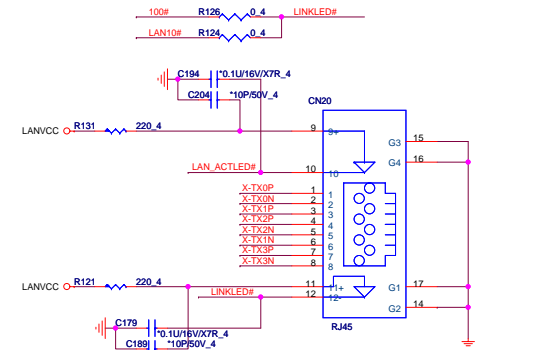
Placed near PHY chip



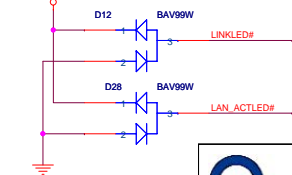
EB1213-0029




EB1213-0030



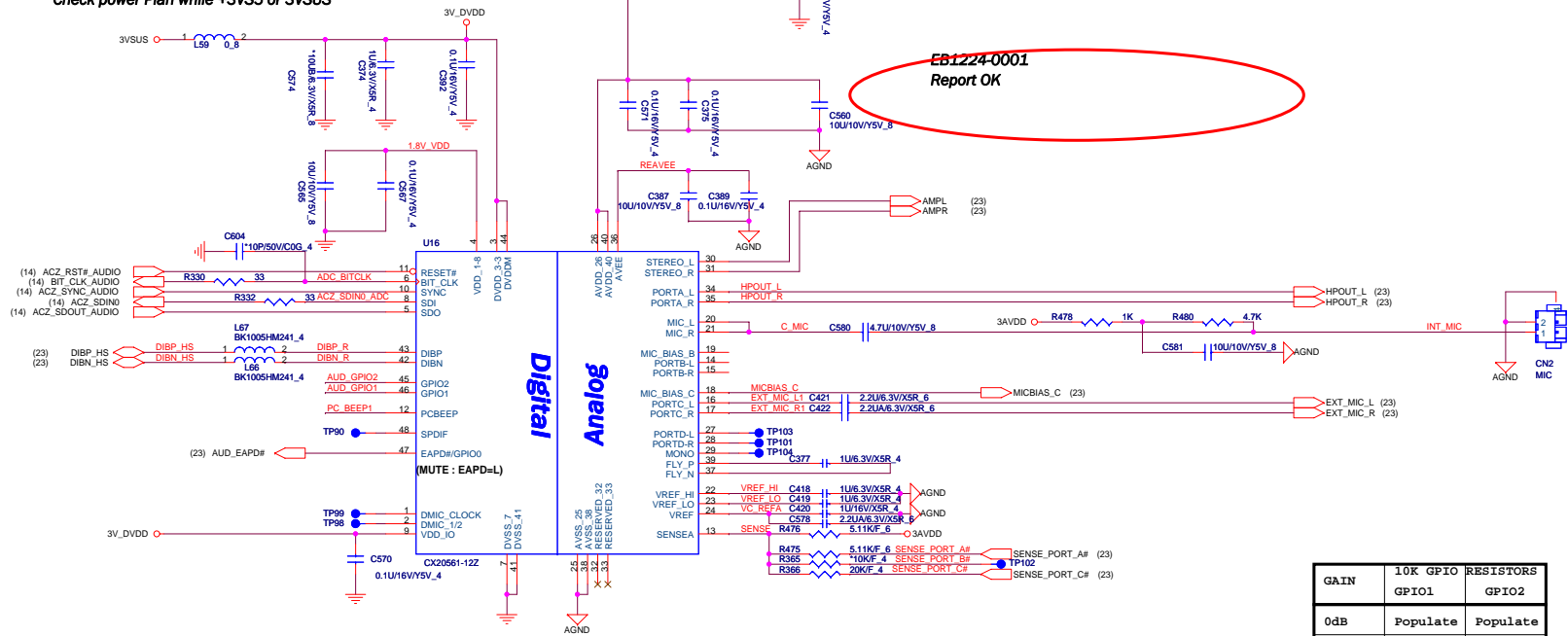
EC0225-0001



	PROJECT : LE6 Quanta Computer Inc.	
	Size C Document Number LAN	Rev 1A

EB1213-0031

Check power Plan while +3VS5 or 3VSUS



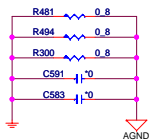
EB1213-0032

Check power Plan while +1.5VS5 or 1.5VSUS

GAIN	10K GPIO GPIO1	RESISTORS GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

STEREO	INTERNAL SPEAKERS
PORT-A	EXTERNAL HEAD-PHONE
MIC	INTERNAL MIC
PORT-B	EXTERNAL MIC

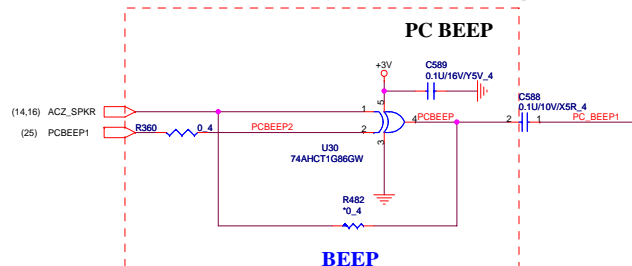
FOR EMI SOLUTION



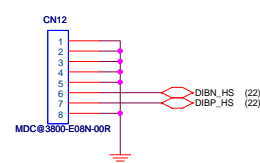
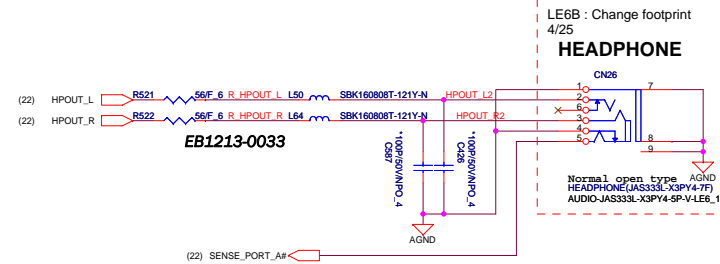
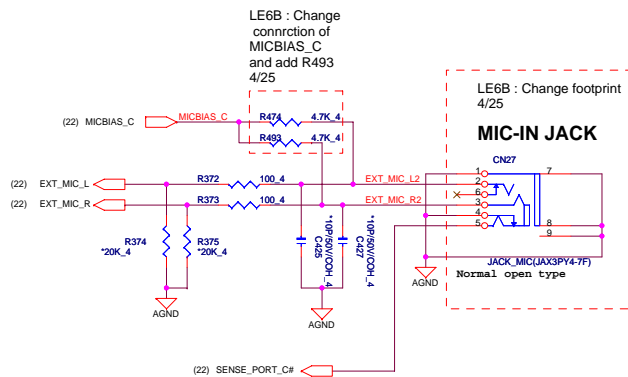
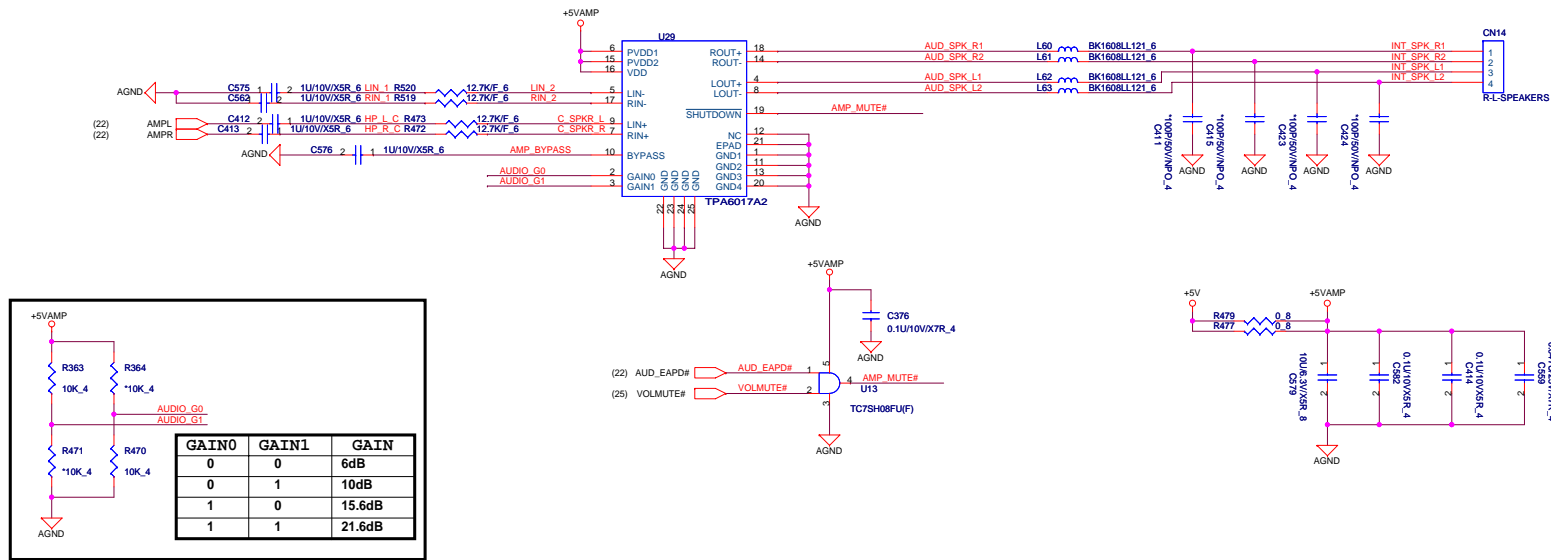
Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2

A circuit diagram showing two parallel resistors, R293 and R292, connected to AUD_GPIO2 and AUD_GPIO1 respectively, both leading to a common ground point labeled *10K_4.

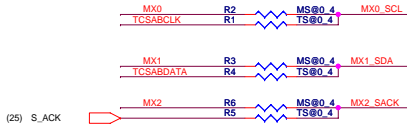
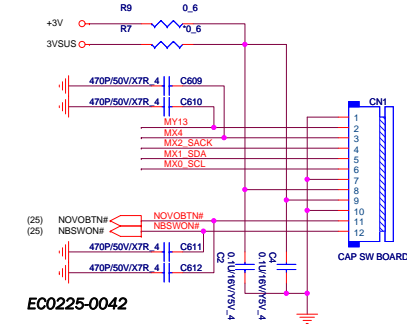
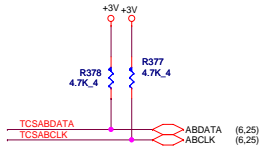
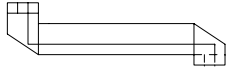
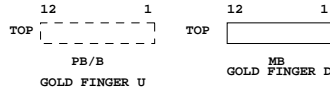
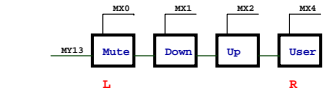
LE6B:Add R360 and change U30 to OR gate base on customer request



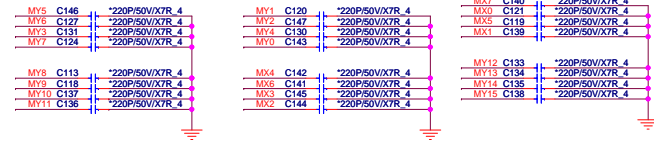
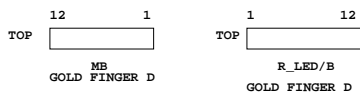
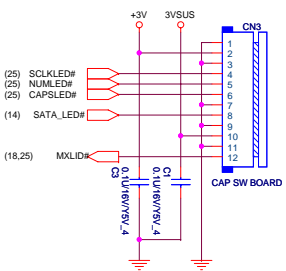
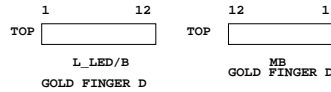
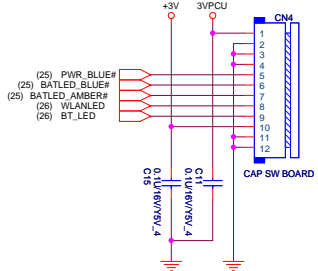
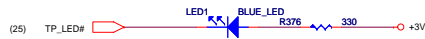
INTERNAL SPEAKER AMPLIFIER



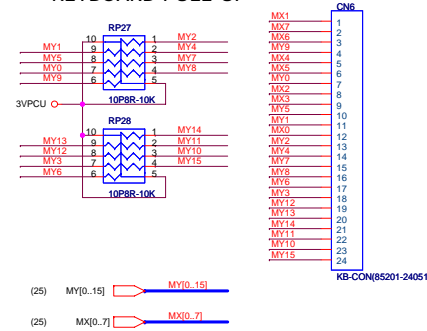
Modem connector



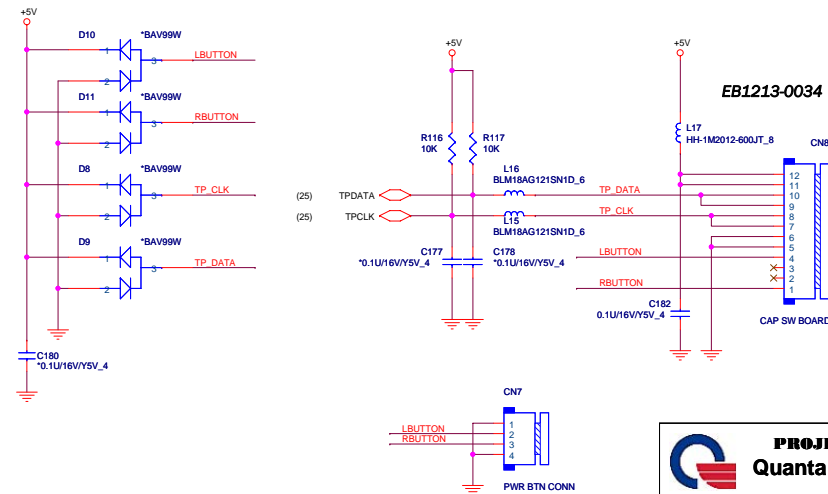
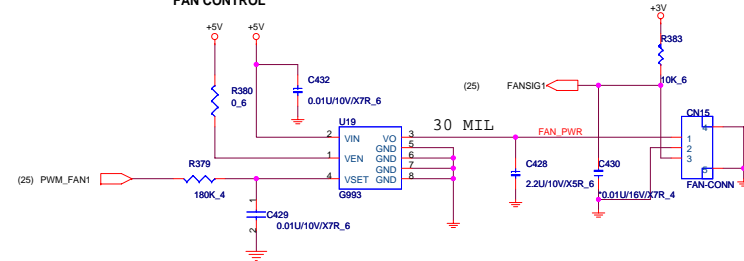
check EC and Vendor for CTS
EB1213-0022

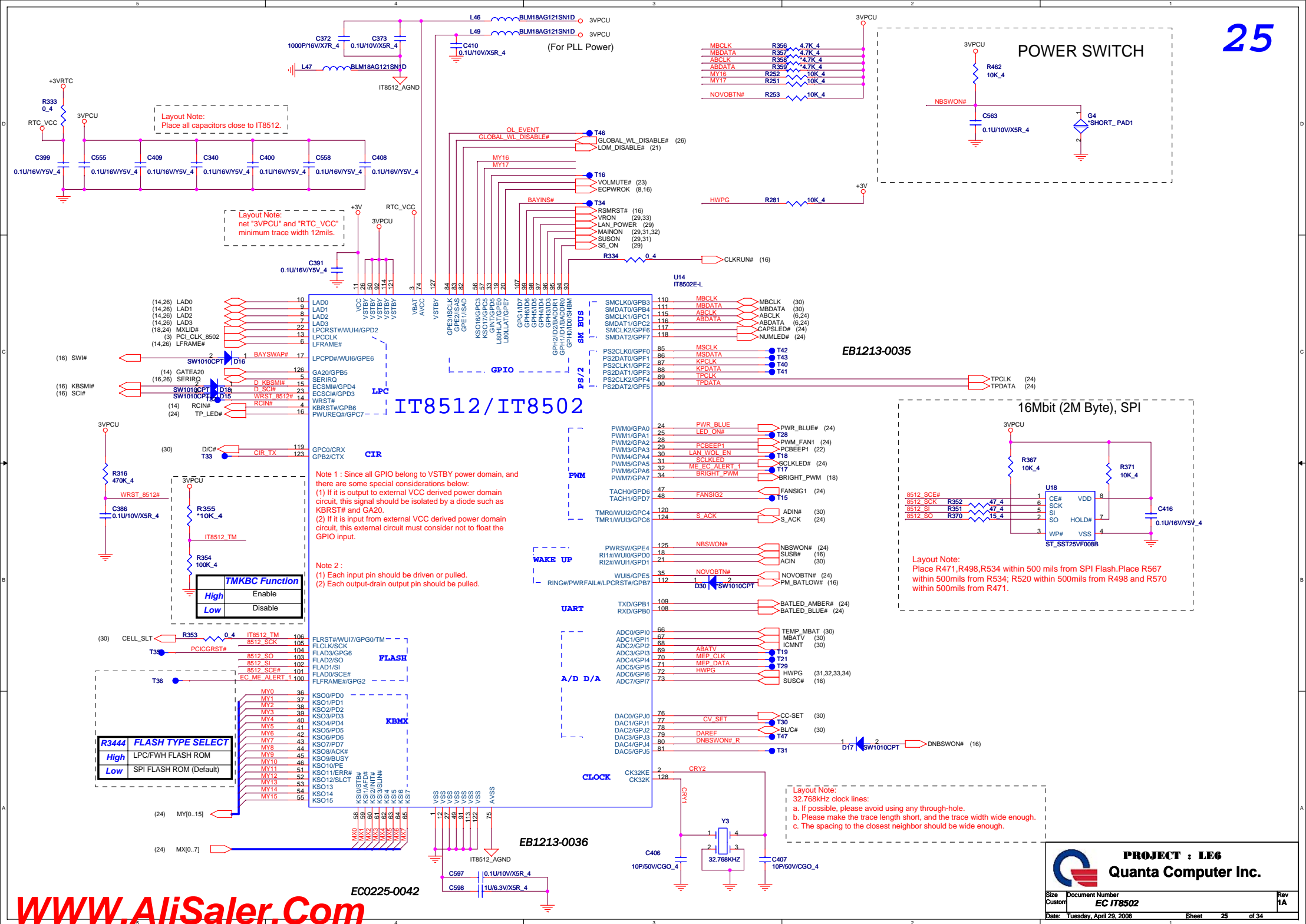


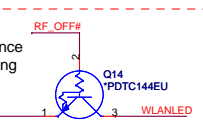
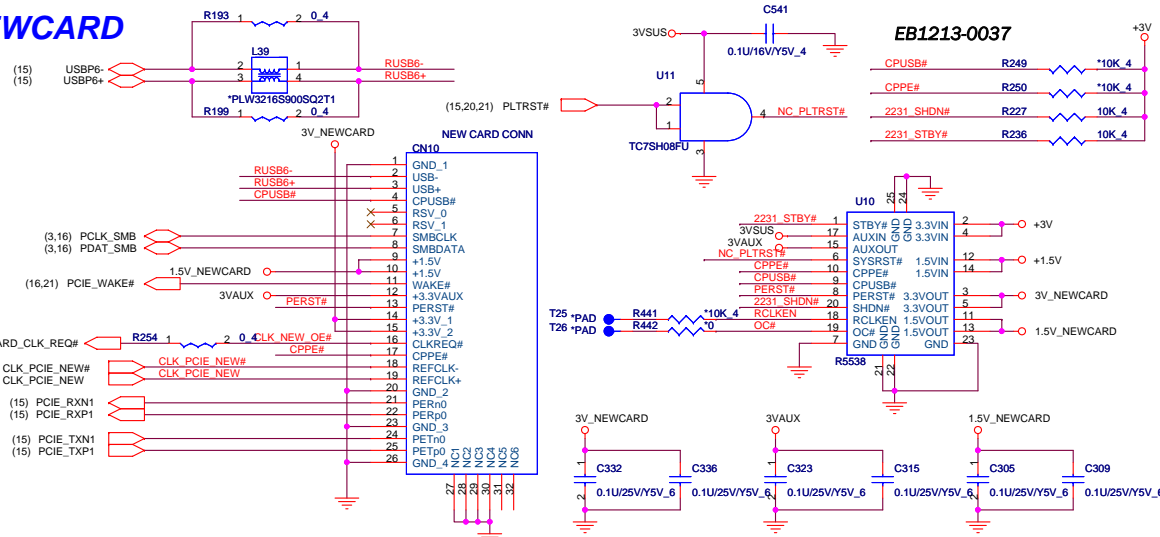
KEYBOARD PULL-UP



FAN CONTROL



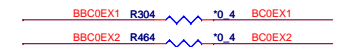




BLUETOOTH

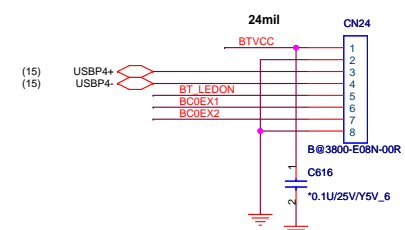
EB1213-0039

Del R315, R463

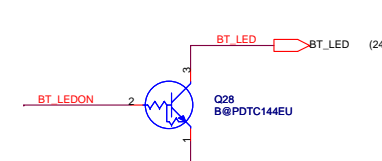


EB1213-0038

Del Q14 and Q30

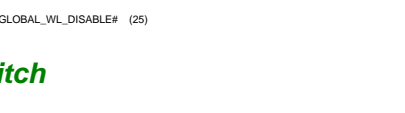


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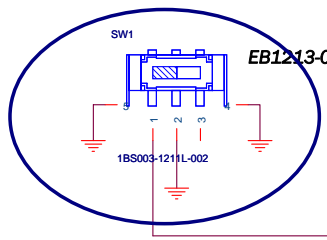


EB1213-0040

Del Q14 and Q30



EB1213-0042



Wireless switch

PROJECT : LE6

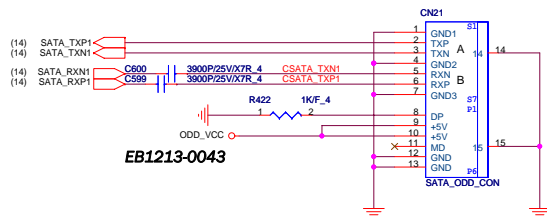
Quanta Computer Inc.

Size Document Number

Custom New Card/Bluetooth/Mini Card

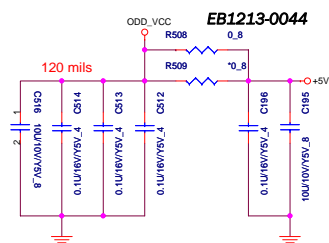
Date: Friday, May 02, 2008 Sheet 26 of 34

**SATA_1
CONNECTOR**



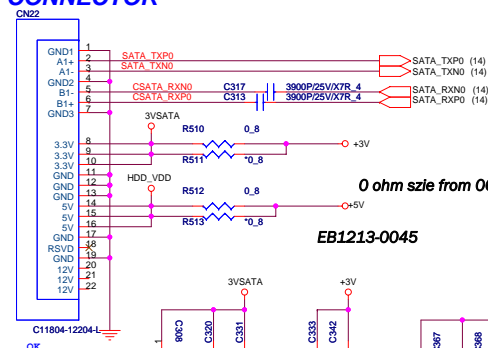
EB1213-0043

0 ohm szie from 0603 to 0805



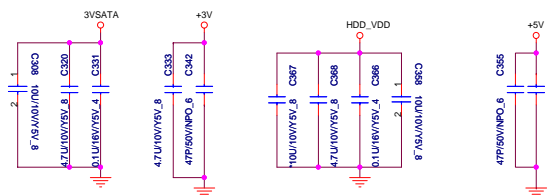
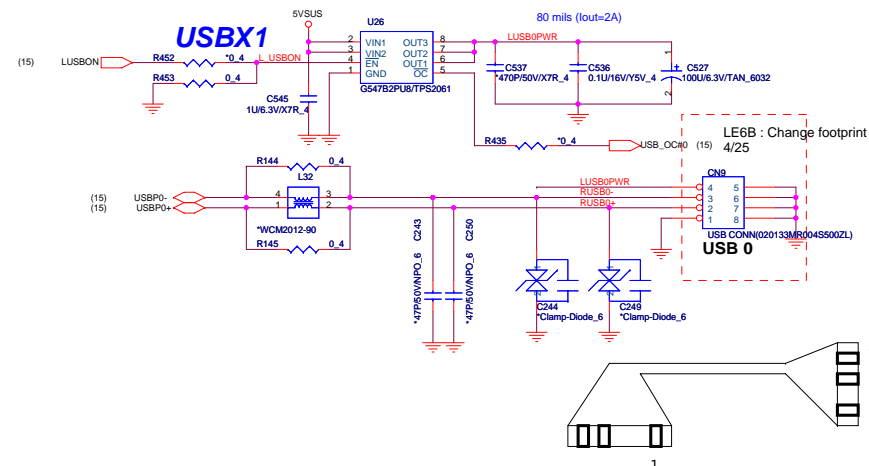
0 ohm szie from 0603 to 0805

EB1213-0045

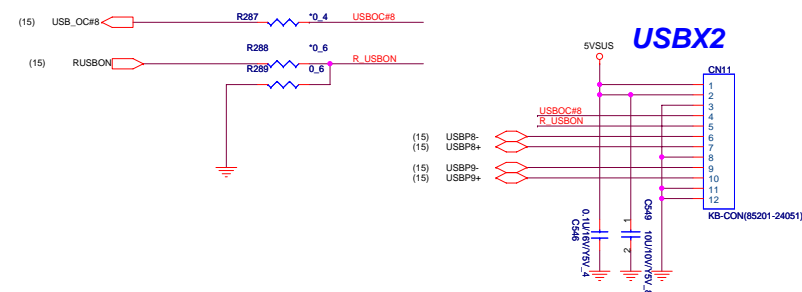


0 ohm szie from 0603 to 0805

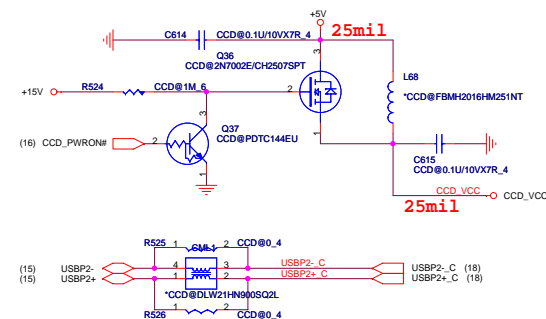
EB1213-0045

**USBX1**

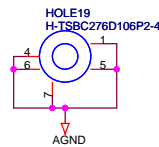
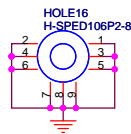
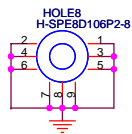
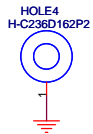
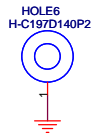
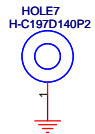
USBX2



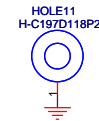
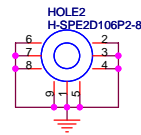
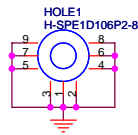
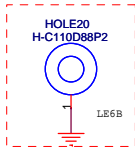
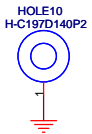
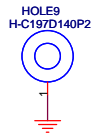
CCD MODULE



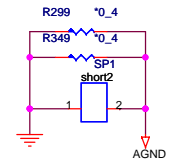
CCD_PWRON#	High Disable	Low Enable
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TOP FAN

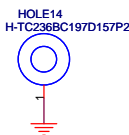
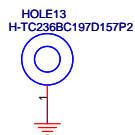
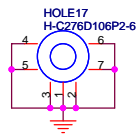
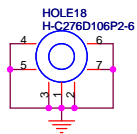


EB1213-0019



CPU

EB1221-0001



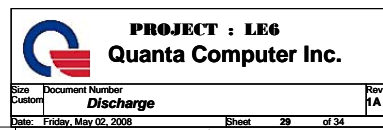
MINI-PCIE

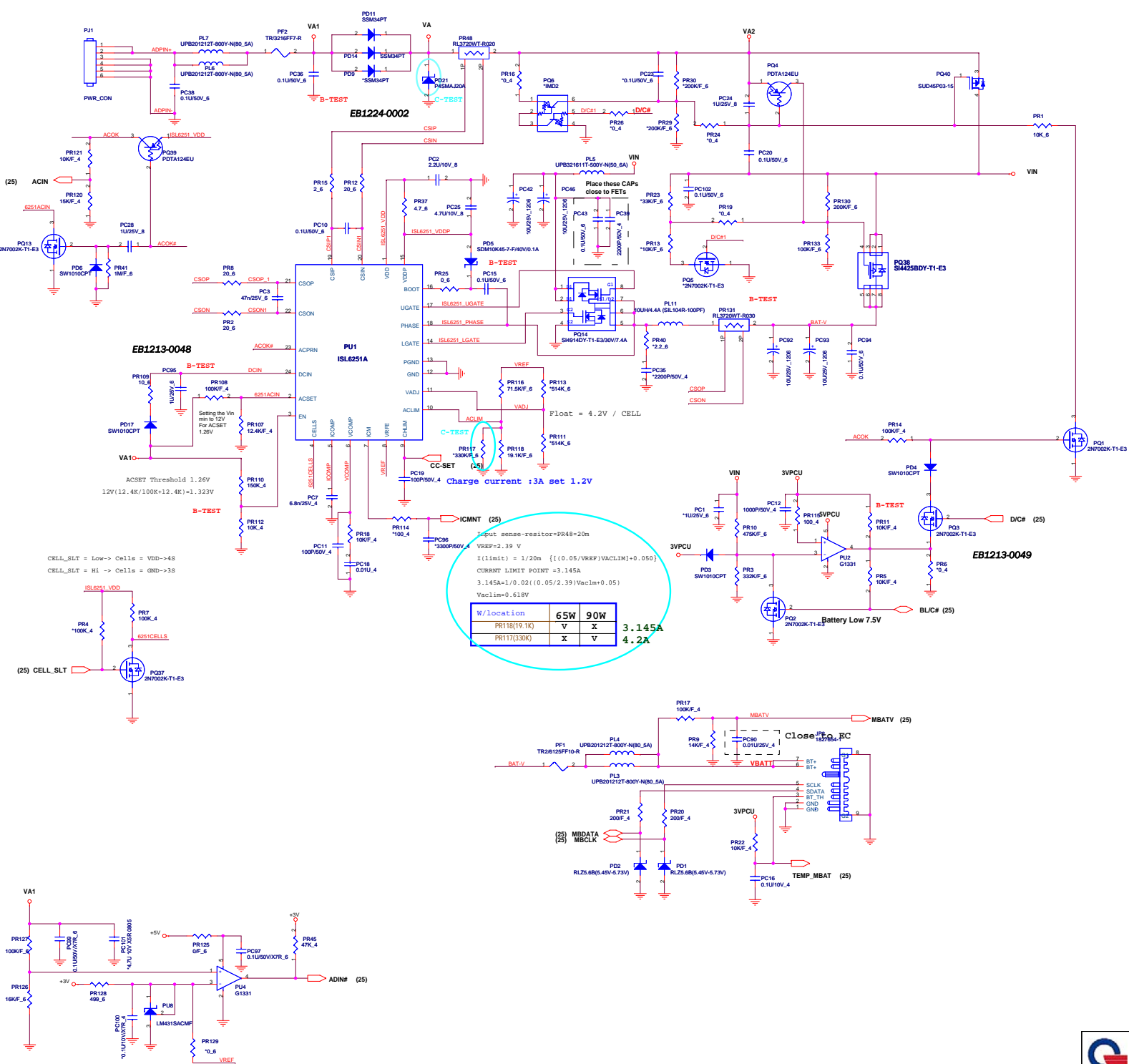
USB
EB1224-0001

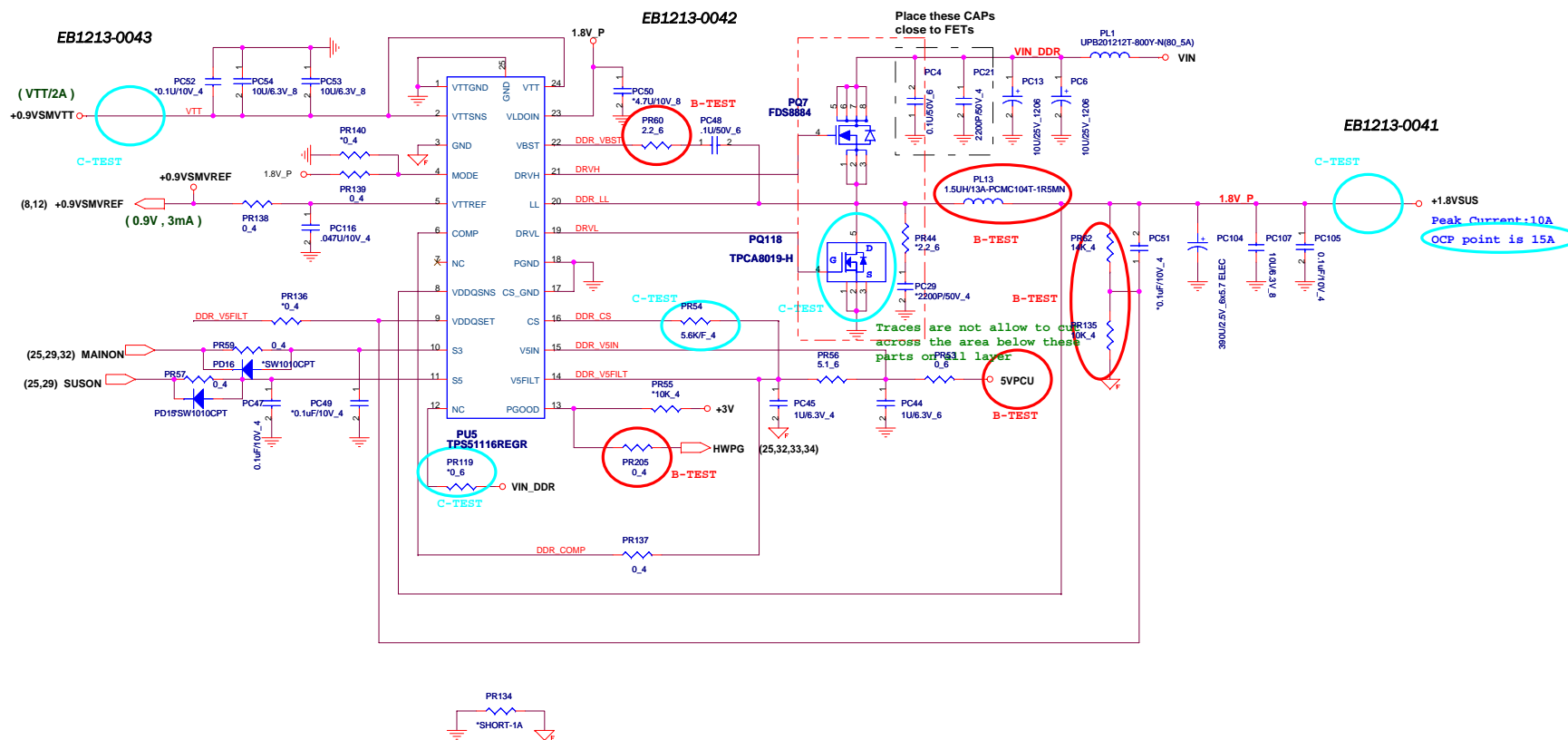
RSPKR

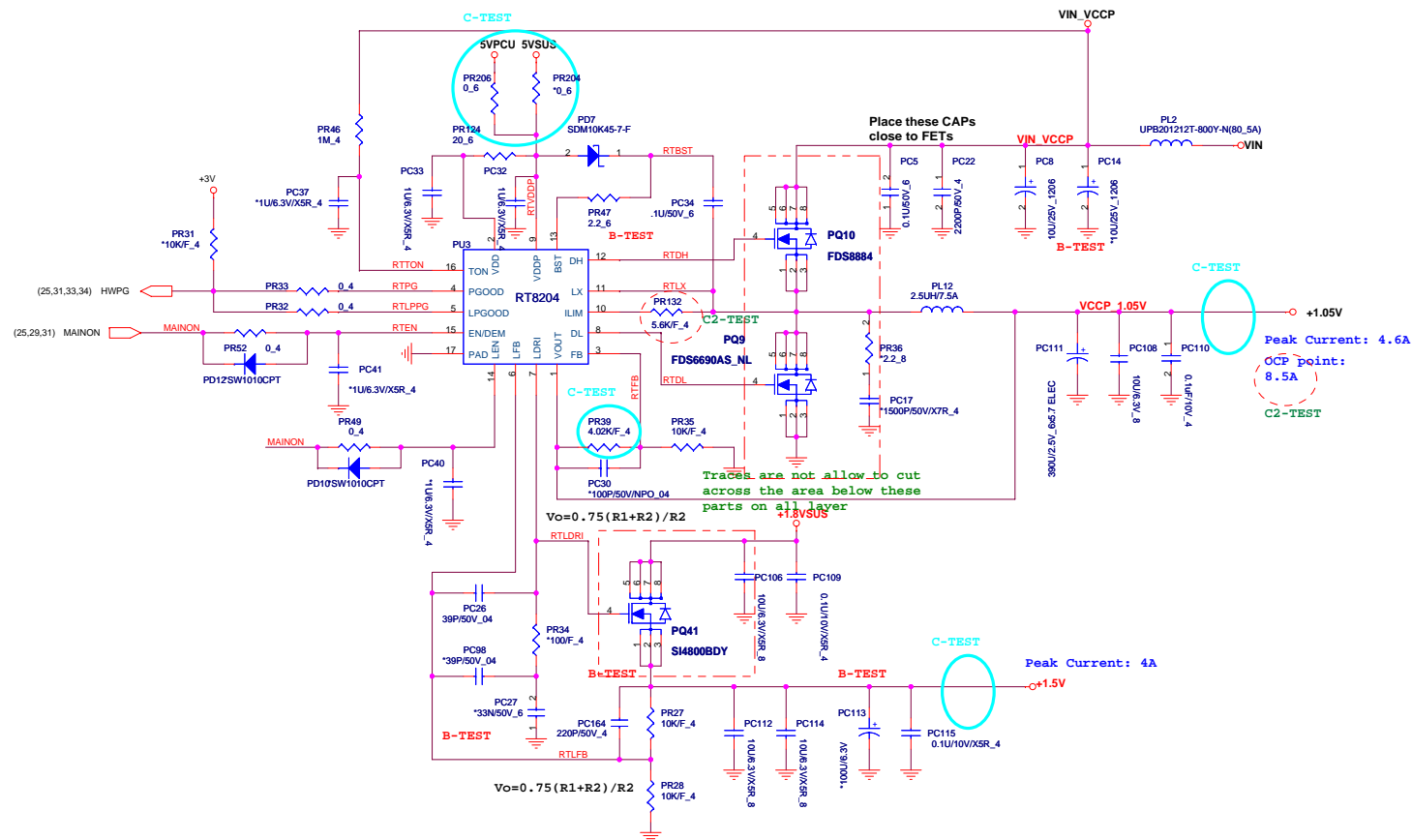
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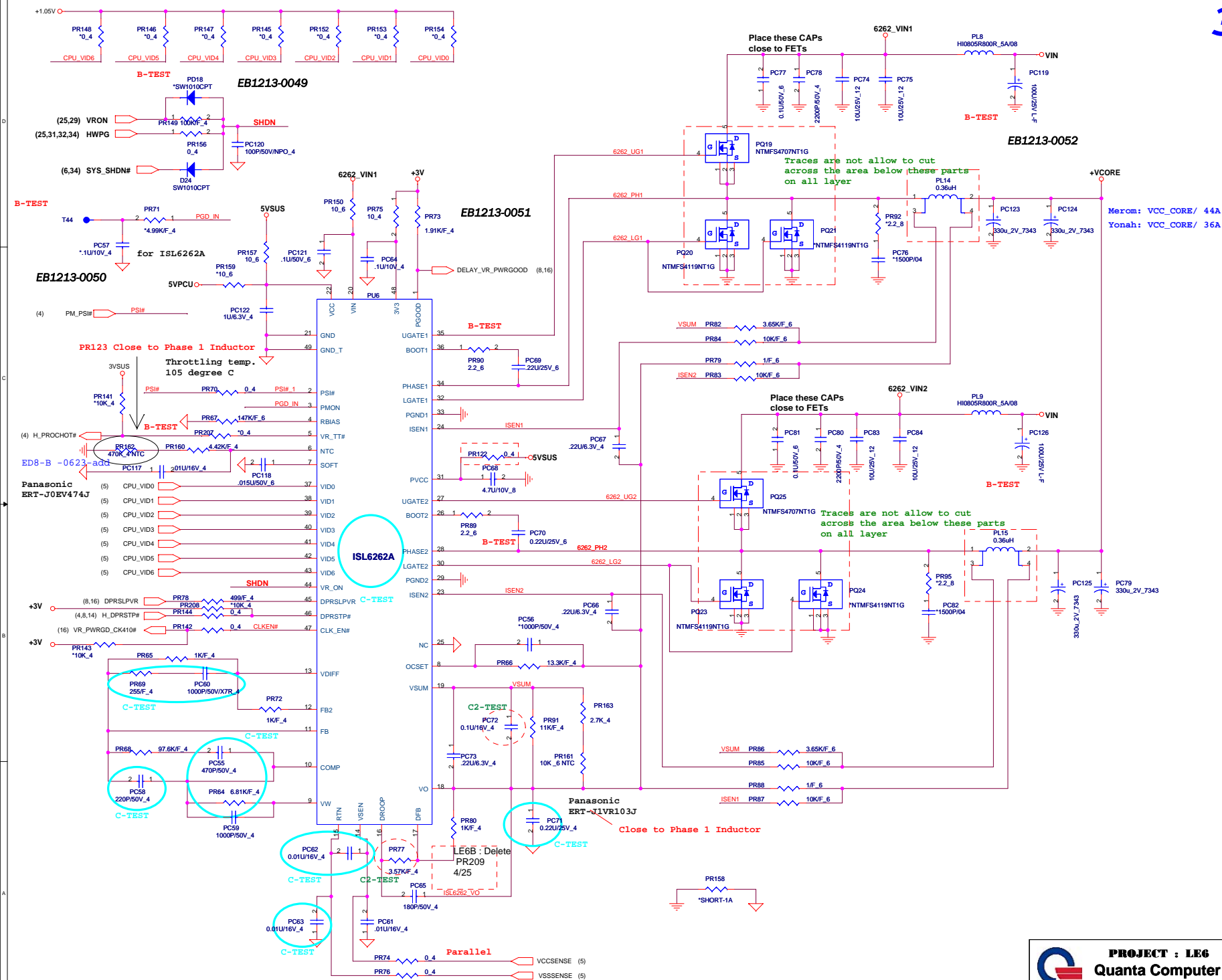
BOT NB











DC/DC 3VPCU/5VPCU/+15V

Ton:OUT1/OUT2 Switching Frequency
VCC: 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

